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Application Number	09/662,358
Filing Date	09/15/2000
First Named Inventor	Taiji NODA et al.
Group Art Unit	2814
Examiner Name	Anh D. Mai
Total Number of Pages in This Submission	
Attorney Docket Number	740819-423

ENCLOSURES *(check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment / Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Assignment Papers *(for an Application)*
- ☐ Drawing(s)
- ☐ Declaration and Power of Attorney
- ☐ Licensing-related Papers
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- ☐ Petition to Convert to a Provisional Application
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Remarks

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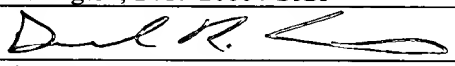
SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm *or* Individual name	Donald R. Studebaker, Reg. No. 32,815 Nixon Peabody LLP 401 9th Street, N.W. Suite 900 Washington, D.C. 20004-2128
Signature	
Date	February 15, 2005

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	
Taiji NODA et al.	)	Group Art Unit: 2814
Application No. 09/662,358	)	Examiner: Anh D. Mai
Filed: September 15, 2000	)	Confirmation No. 1724
For: METHOD FOR FABRICATING A SEMICONDUCTOR DEVICE HAVING A POCKET DOPANT DIFFUSED LAYER (AS AMENDED)	)	Date: February 15, 2005

REQUEST FOR RECONSIDERATION

Mail Stop **Non Fee Amendment**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Official Action dated November 15, 2004, it is respectfully requested that the rejections of record be reconsidered and withdrawn by the Examiner in view of the following comments. As previously, claims 1-10, 12, 15, 21, 23 and 24 are presently pending in the instant application with claims 1-5 being withdrawn from further consideration by the Examiner.

With reference now to the Official Action and particularly paragraph 3 thereof, claims 6-10, 12, 21, 23 and 24 have been rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,650,340 issued to Burr et al., in view of U.S. Patent No. 5,786,620 issued to Richards, Jr., et al. and U.S. Patent No. 5,970,353 issued to Sultan. This rejection is respectfully traversed in that the combination proposed by the Examiner neither discloses nor remotely suggests that which is presently set forth by Applicants' claimed invention.

In reviewing Applicants' claimed invention, independent claim 6 recites a method for fabricating a semiconductor device comprising the first step of forming a gate electrode, a second step of implanting indium ions into the semiconductor region on both sides of the electrode using the gate electrode as a mask, a third step of implanting ions of a first dopant into the semiconductor region into which an amorphous layer has been formed, and a fourth step of conducting a first annealing process to active the first and second implanted layers, thereby forming an extended high concentration dopant diffused layer of the first conductivity type through diffusion of the first dopant and a pocket dopant diffused layer of the second conductivity type which is in contact with a bottom portion of the extended high concentration dopant diffused layer through diffusion of the indium ions wherein in the second step, with a dislocation loop layer being formed in the lower region of the amorphous layer in the semiconductor region due to the heavy ion implantation, in the fourth step, the pocket dopant diffused layer being formed having a peak dopant concentration produced by trapping indium ions in the dislocation loop layer, the pocket dopant diffused layer and the extended high concentration dopant diffused layer being in contact at the peak dopant concentration of the pocket dopant diffused layer, and a side of the extended high concentration dopant diffused layer located below the gate electrode, it is not covered by the pocket dopant diffused layer and an implant dose of the indium ions is more than $5x10^{13}/cm^2$.

More specifically, the present invention as set forth in independent claim 6 as well as those claims which depend therefrom recite features which are not disclosed in nor suggested by the prior art of record. Particularly, as the Examiner can readily appreciate, independent claim 6 sets forth that an amorphous layer and a dislocation loop are formed in a semiconductor region by implanting indium ions as heavy ions at an implant dose of $5x10^{13}/cm^2$ or more, that a pocket dopant diffused layer is formed having a peak pocket

dopant concentration produced by trapping heavy ions in the dislocation loop layer, and the pocket dopant diffused layer and the extended high concentration dopant diffused layer are in contact at the peak dopant concentration of the pocket dopant diffused layer. Again, it is respectfully submitted that the prior art combination proposed by the Examiner fails to disclose or suggest such features.

Specifically, in rejecting in Applicants' claimed invention, the Examiner asserts that Burr has been shown to teach all the features of the claimed invention with the exception of implanting heavy ions into the semiconductor region on both sides of the gate electrode and the dose of indium heavy ions to be more than $5x10^{13}/cm^2$ although the dose of $5x10^{13}/cm^2$ of Burr meets the lower limit of the claimed dose. In deed, as appreciated by the Examiner, $5x10^{13}/cm^2$ is an upper limit dose set forth in Burr whereas it is a lower limit dose of the present invention. The present invention, however, not only defines dose as an implant condition but also defines dose so as to form an amorphous layer and a dislocation loop layer in a semiconductor region. That is, even if indium ions are implanted in an upper limit dose of $5x10^{13}/cm^2$ in Burr, Burr does not disclose the claimed invention unless an amorphous layer and a dislocation loop layer were formed in the semiconductor region as is the case with the present invention.

Further, in rejecting Applicants' claimed invention, the Examiner asserts in the Office Action that Sultan discloses that the amorphizing dose of indium is $1x10^{14}/cm^2$ or more and a pocket diffusion layer 62 is formed. While this reference may disclose that the amorphizing dose set forth as $1x10^{14}/cm^2$ or more, this reference fails to disclose forming a pocket diffusion layer. Region 62 which the Examiner refers to as the pocket diffusion layer is actually the interstitial formed in the extension regions 62 and 67 as illustrated in Fig. 14 of the reference. Clearly, this is not a pocket diffusion layer. Furthermore, Sultan fails to

disclose amorphizing the interstitial regions 62 at an indium ion dose of $1x10^{14}/cm^2$ or more. The interstitial regions 62 are formed at 10 to 30% of the amorphous dose, that is, $1x10^{13}$ to $3x10^{13}/cm^2$ as noted in column 6, lines 8-10 and 14-17. Accordingly, the Sultan reference discloses forming the interstitial regions 62 at 10 to 30% of the amorphous dose in order to avoid being amorphized which is directly contrary to that which is presently set forth by Applicants' claimed invention. With respect to the teachings of Richards, Jr. et al., while this reference may disclose reducing the short channel effects on both source and drain implants, this reference clearly fails to overcome the aforementioned shortcomings associated with each of the Burr and Sultan references relied on by the Examiner. More specifically, as noted hereinabove, Sultan fails to disclose a pocket diffusion layer and therefore it is respectfully submitted that the combination of such teachings with Burr as proposed by the Examiner is not proper. Further, Sultan fails to disclose or suggest forming an amorphous layer and a dislocation loop layer in a semiconductor region. Hence, the claimed invention as set forth in independent claim 6 clearly distinguishes over the combination proposed by the Examiner and is in proper condition for allowance.

With respect to the Examiner's assertion on pages 4 and 5 of the Official Action that Applicants' specification contains no disclose of either the critical nature of the claimed dose of more than $5x10^{13}/cm^2$ or any unexpected results arising therefrom, Applicants wish to direct the Examiner's attention to pages 19 and 20 of Applicants' specification wherein it is specifically recited that the indium ions are implanted at an implant dose of about $1x10^{14}/cm^2$. However, if the ions are implanted at an implant dose of $5x10^{13}/cm^2$ or more, then the amorphous layer can be formed inside the semiconductor substrate 100 and the segregated parts of the indium can be formed in the pocket dopant diffusion layer 106. Cleary, Applicants' specification provides not only adequate support for the limitations set

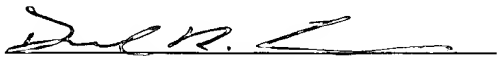
forth in independent claim 6 but also notes the critical nature of the claimed dose resulting in the amorphous layer being formed inside the semiconductor substrate and the segregated parts of the indium being formed in the pocket dopant diffusion layer. Accordingly, it is respectfully submitted that Applicants' claimed invention as set forth in independent claim 6 as well as those claims which depend therefrom clearly distinguish over the combination proposed by the Examiner and are in proper condition for allowance.

With respect to claims 7-10, 12, 15, 21, 23 and 24, each of these claims are either directly or indirectly dependent on claim 6 and include all of the limitations set forth therein. Accordingly, it is respectfully submitted that these claims are likewise in condition for allowance for at least the reasons set forth hereinabove.

Therefore, it is respectfully requested that the rejections of record be reconsidered and withdrawn by the Examiner, that claims 6-10, 12, 15, 21, 23 and 24 be allowed and that the application be passed to issue.

Should the Examiner believe a conference would be of benefit in expediting the prosecution of the instant application, he is hereby invited to telephone counsel to arrange such a conference.

Respectfully submitted,



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